Title: SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR TESTING SEMICONDUCTOR MEMORY DEVICE Inventor: Yuji NAKAGAWA Application No. New Docket No. 108075-00112 Memory Core wl-timing 79 ref-req Memory Control Circuit Refresh Timer test mtd 76 cep web oep ad0 ad1 75 73 Buffer Buffer Buffer Buffer Buffer Input Input Input 65 Input Input -64 -62 -63 61 **A**0 A1 Control Signal CTL

Address Signal ADD

Fig.1 (Prior Art

20

#### Fig.2(Prior Art)

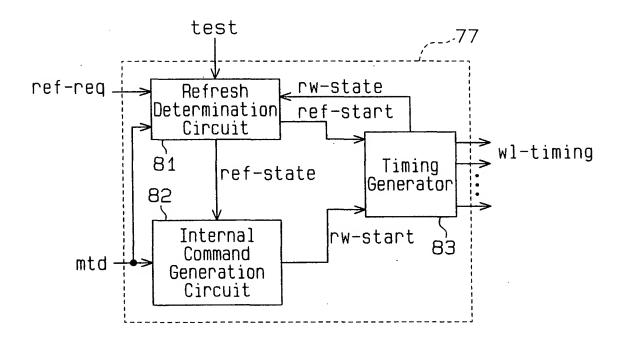
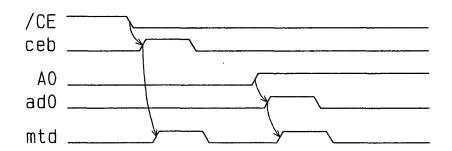
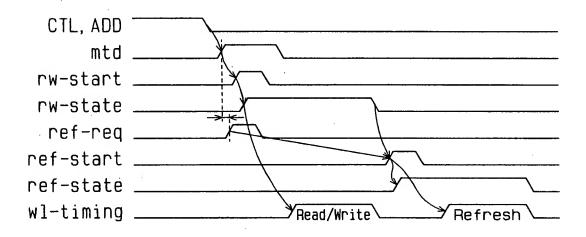


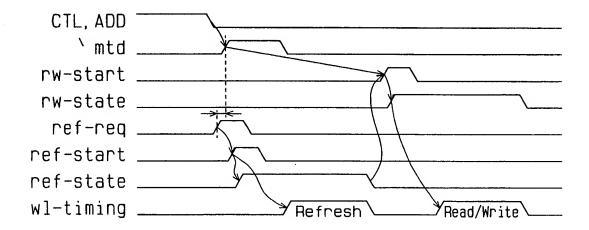
Fig.3(Prior Art)



## Fig.4(Prior Art)



#### Fig.5 (Prior Art)



## Fig.6(Prior Art)

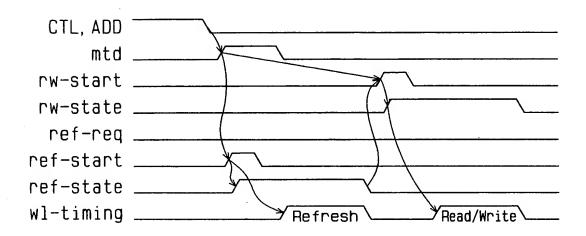
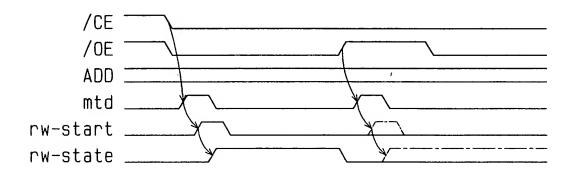


Fig.7 (Prior Art)



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# Fig 8 (Prior Art)

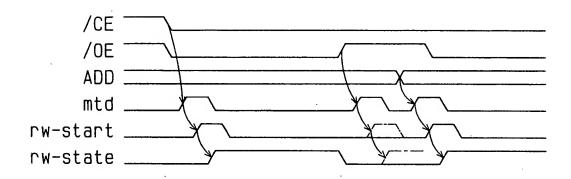
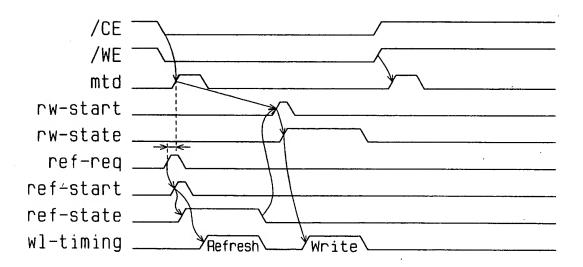


Fig.9(Prior Art)



#### Fig.10(Prior Art)

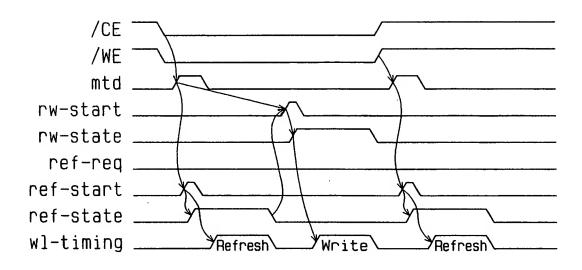
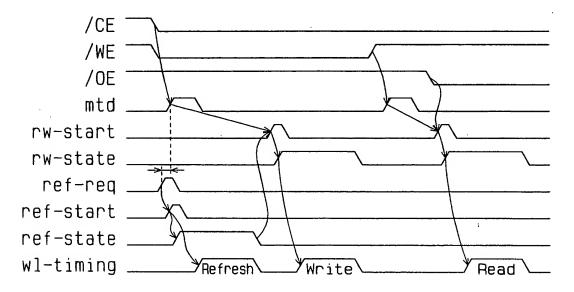
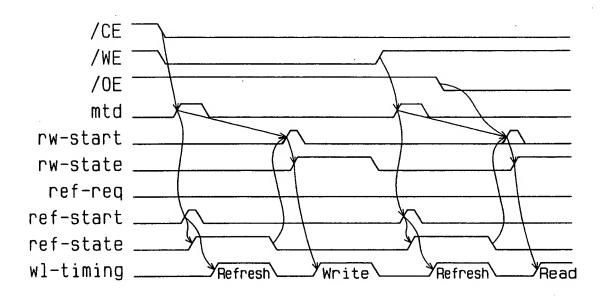
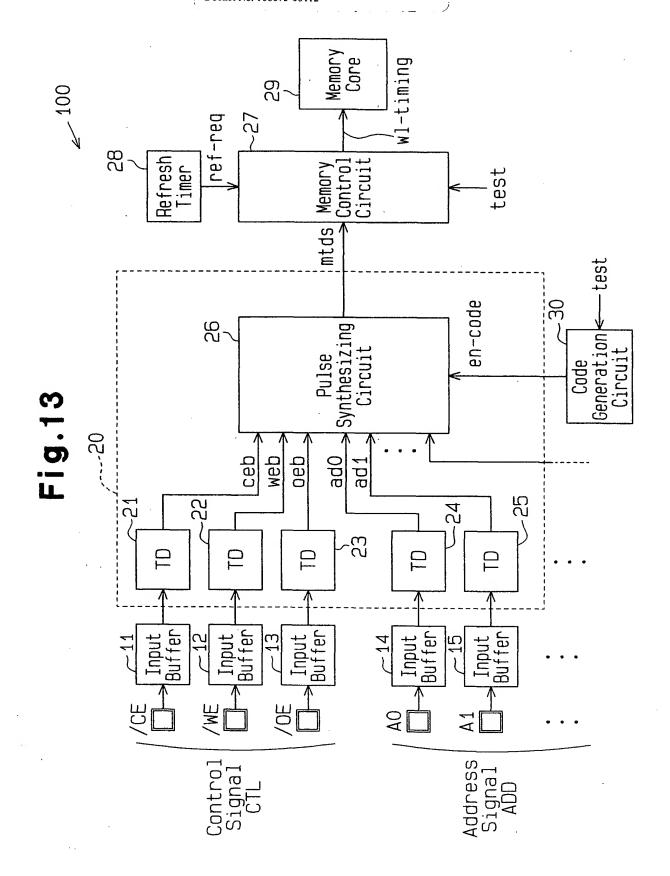


Fig.11 (Prior Art)



# Fig.12 (Prior Art)





26e 26b 26c , en-ceb • oeb en-web en-oeb en-ad0 Ceb ,22 Delay De lay De lay Delay 23.7

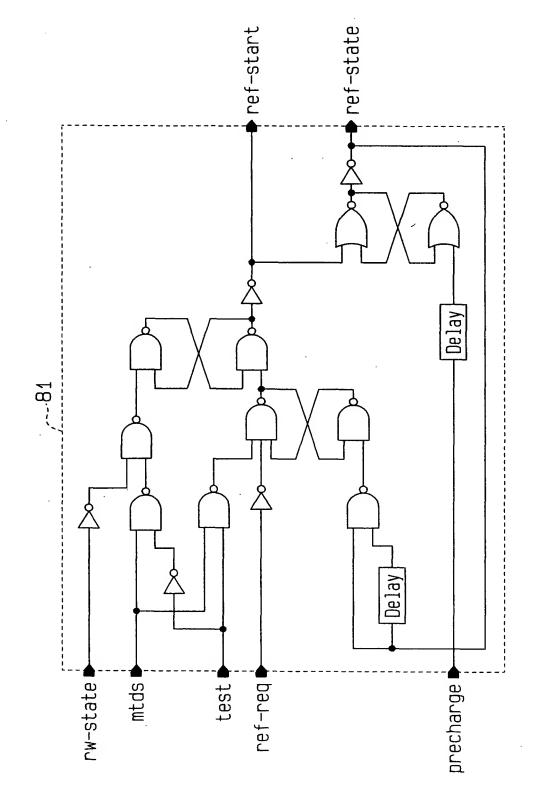


Fig. 15

Fig.16

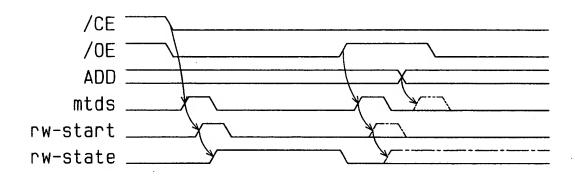
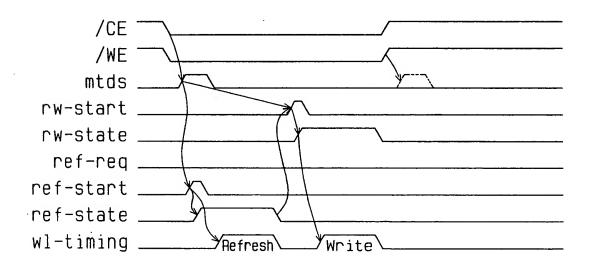


Fig.17



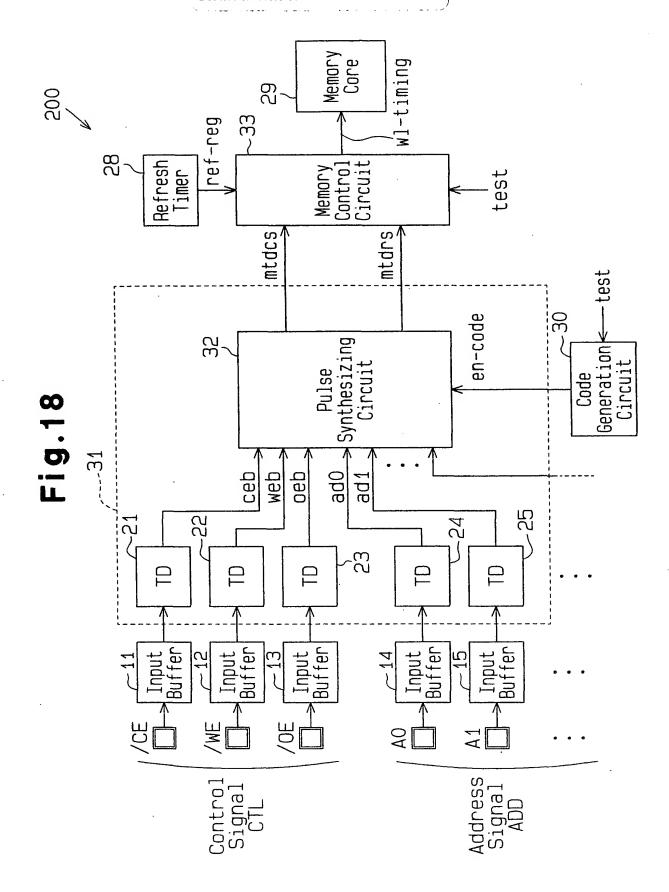
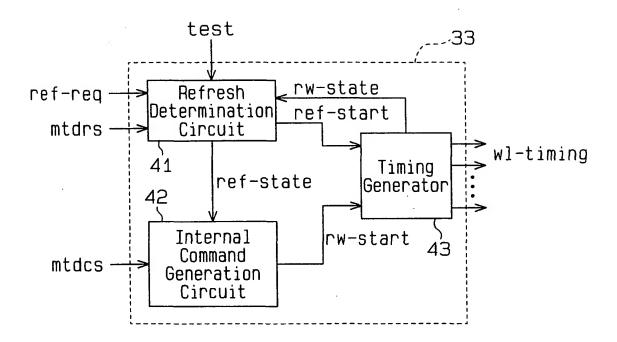
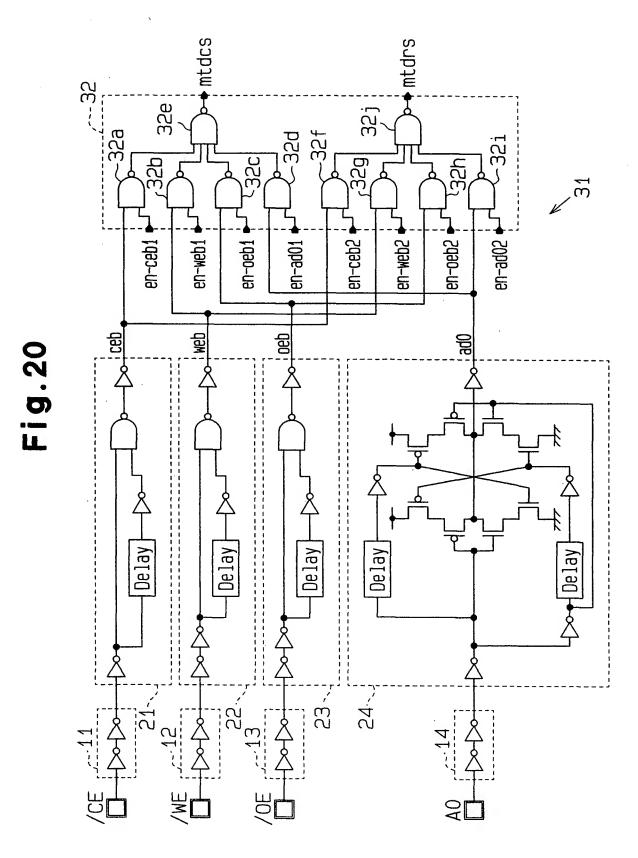
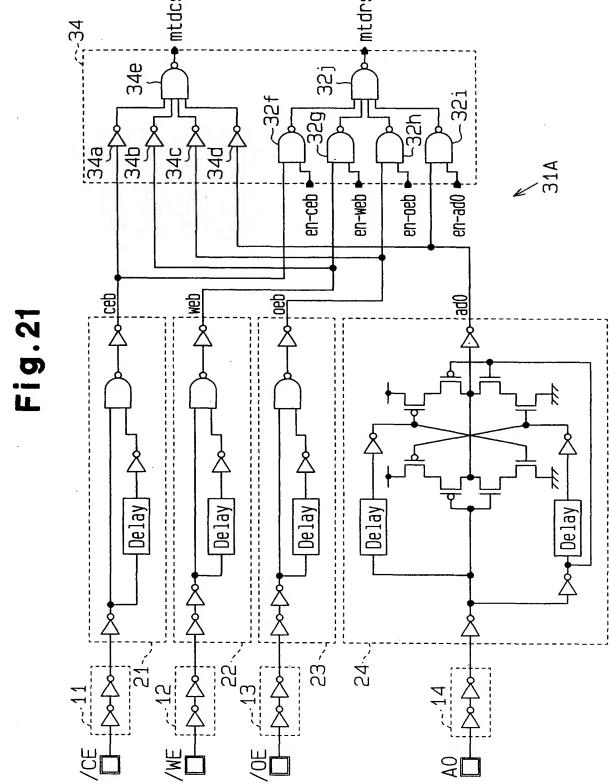


Fig.19



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Fig 22

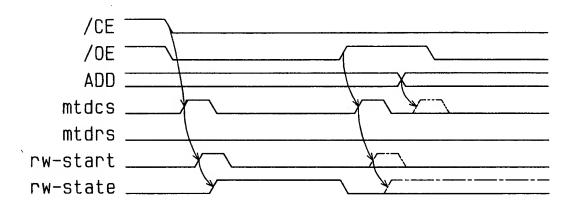


Fig. 23

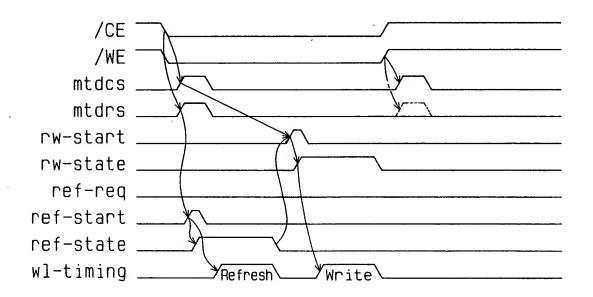


Fig 24

